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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/372,879	08/12/1999	STEFANOS SIDIROPOULOS	RD-036	1940

27846 7590 07/18/2002

RAMBUS INC.
4440 EL CAMINO REAL
LOS ALTOS, CA 94022

EXAMINER

FARAHANI, DANA

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 07/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/372,879

Applicant(s)

SIDIROPOULOS ET AL.

Examiner

Dana Farahani

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 May 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-37 is/are pending in the application.
- 4a) Of the above claim(s) 25 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-37 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al., hereinafter Lee (U.S. 6,329,694), previously cited.

Lee discloses, figure 14, an integrated circuit device comprising: a conductive pad (I/O pad) to receive an input signal from an external signal line; a first doped region 61 of the first conductivity type disposed in a semiconductor substrate 50 of a second conductivity type, underlying and surrounding the conductive pad; a conductive region 65 of the first conductivity type disposed in the first doped region 61; a first tap region 66 spaced apart from and surrounding a substantial portion of the first doped region, wherein the first tap region is electrically coupled to a first supply voltage Vss; an output driver transistor, comprising segments 52, 53, and 54, having a drain region 54 and a

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source region 53, wherein the drain region is electrically coupled to the conductive pad; and a second tap region 66 surrounding the output driver transistor, wherein the second tap region is electrically and physically coupled to a second supply voltage V_{ss} and the source region.

Regarding claim 2, the first and second supply voltages are ground (V_{ss}).

Regarding claim 3, first tap region completely surrounds the first doped region.

Regarding claim 4, the first tap region is a discontinuous region.

Regarding claim 5, the doping concentration of the first doped region 61 is less than the doping concentration of the conductive region 65.

Regarding claim 6, the first tap region is a third doped region and the second tap region is a fourth doped region.

Regarding claim 7, the third doped region is of an opposite conductivity type than the first doped region.

Regarding claim 8, the fourth doped region is a P type doped region.

Regarding claim 9, a portion of the first tap region is decoupled from the first supply voltage to provide a predetermined equivalent series resistance between the first doped region and the first supply voltage.

Regarding claim 10, the first tap region substantially surrounds the first doped region.

Regarding claim 11, the first tap region is a discontinuous region.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 12-22 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee.

Regarding claim 12, Lee discloses the bond pad comprising conductive bonding layers 63-65; a first doped region 61 of the first conductivity type formed in semiconductor substrate 50 of the second conductivity type, underlying and surrounding the conductive bonding layer; a conductive region 65 of the first conductivity type disposed in the first doped region, the conductive region having a surface area; and a conductive tap region 66 spaced apart from and surrounding at least a portion of the first doped region, wherein a portion of the conductive tap region is electrically coupled to a supply voltage.

Lee does not disclose the surface region 65 substantially equal to the surface area of the conductive bonding layer. It would have been within the level of ordinary skill in the art to change the size of the region 65.

Regarding claim 13, the supply voltage is a ground voltage and the conductive bonding layer includes a metal (see column 4, lines 40-55).

Regarding claim 14, the doping concentration of the first doped region is less than the doping concentration of the conductive region.

Regarding claim 15, the conductive tap region is a third doped region and is of an opposite conductivity type than the first doped region.

Regarding claim 16, a portion of the conductive tap region is decoupled from the supply voltage to provide a predetermined equivalent series resistance between the doped region and the supply voltage.

Regarding claim 17, the conductive tap region is a continuous region.

Regarding claim 18, the conductive tap region substantially surrounds the doped region.

Regarding claim 19, the conductive tap region is a discontinuous region.

Regarding claim 20, the conductive tap region substantially surrounds the doped region in a concentric-like manner.

Regarding claim 21, the conductive region is polysilicon.

Regarding claim 22, the conductive tap region is a doped layer positioned beneath the conductive region.

Regarding claim 28, Lee discloses in figure 10, a plurality of source regions 13 and 23, where one of the source region of the plurality of source regions being electrically and physically coupled to the conductive tap region 25; a plurality of drain regions 24 and 14, where one of the drain region of the plurality of drain regions being electrically coupled to the bond pad; and wherein the conductive tap region is spaced proximal to and surrounds at least one drain region 24 of the plurality of drain regions.

Although, Lee does not disclose the other drain and source regions are connected to the Vcc, or ground pad, it is well known in the art to ground either source or drain of a MOSFET transistor in order to interchange the source and the drain regions.

5. Claims 23, 24-27, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of the Japanese patent to Sakai et al. (document ID# 60000769), newly cited.

Regarding claims 23 and 29, Lee discloses transistor layout 22 in the circuit device in figure 14 having a bond pad (I/O), the transistor layout comprising a drain region 54 of the first conductivity type formed in a semiconductor substrate 50 of the second conductivity type, the drain region being electrically coupled to the bond pad; a source region 53; and a conductive tap region 55 spaced proximal to and surrounding the drain region, wherein the conductive tap region is electrically coupled to a supply voltage Vss and electrically and physically coupled to the source region.

Lee does not disclose the source and the drain region being of opposite conductivity types.

It would have been obvious to one of ordinary skill in the art to make the source and the drain region of the opposite conductivity type since it was known in the art that both conductivity types could be present in source/drain region (see the Japanese patent, figure 4c).

Regarding claim 24, the supply voltage is coupled to a ground voltage Vss.

Regarding claim 26, the conductive tap region 55 is spaced proximal to and completely surrounds the drain region.

Regarding claim 27, the conductive tap region is a discontinuous region.

Regarding claims 31-37, Lee does not disclose in the embodiment of figure 14 that a tap region spaced proximal to the drain region and electrically decoupled from the supply voltage and the conductive tap region. It would have been within the level of ordinary skill in the art to make region 66 spaced proximal to the drain region and electrically decoupled from the supply voltage and the conductive tap region in order to make the present invention (see figure 15 of Lee).

Response to Arguments

6. Applicant's argument that the position of I/O pad is not shown relative to n-well 61 is not found persuasive for the following reason. As can be seen clearly from the figure, n-well 61 is underlying, and at least surrounding the lower portions of the I/O pad.

7. Applicant's arguments with respect to claims 12 and 23 have been considered but are moot in view of the new grounds of rejection.

Conclusion

This action is made **NON-FINAL**. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (703)305-1914. The examiner can normally be reached on M-F 8:00AM - 5:00PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703)306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9318 for regular communications and (703)872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Dana Farahani
July 12, 2002



OLIK CHAUDHURI
SUPERVISORY PATENT EXAMINER
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